

ABSTRACT OF THE DISCLOSURE

An array of phase changing memory cells that includes a current source, a voltage sensor, a plurality of conductive bit lines electrically connected to the current source, a plurality of conductive word lines each electrically connected to a ground plane via a first resistor and to the voltage sensor, and a plurality of memory cells. Each memory cell is connected between one of the bit lines and one of the word lines and includes phase change memory material. One of the memory cells is selected by turning on switches just on the bit line and word line connected thereto, or by turning a switch connected in series between the corresponding bit and word lines, where the read current flows through the selected memory cell and the voltage sensor measures a voltage drop across the selected memory cell.

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